

ABSTRACT

A process for forming a transistor having a gate width of less than 70 nm is disclosed herein. The process includes E-beam radiation a gate patterned on a photoresist layer, trimming the gate patterned on the photoresist layer, and

5 etching the gate patterned on the photoresist layer to a polysilicon layer disposed below the photoresist layer. The gate pattern is E-beam eradicated by an electron beam.

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